

IN THE CLAIMS:

The status of the claims is as follows:

Claims 1-11 (Cancelled).

12. (Original) A method of forming an interconnect structure having a first feature and a second feature, comprising the steps of:

(a) providing an article comprising a conductive layer that has a dielectric layer thereon;

(b) depositing a first photoresist layer on the dielectric layer;

(c) patterning the first photoresist layer to form a first mask pattern defining the first feature;

(d) etching the dielectric layer using the first photoresist layer as a mask to form the first feature using an etch chemistry that comprises a member of the group NH_3 , NF_3 and N_2O ;

(e) removing the first photoresist;

(f) depositing a second photoresist layer on the article;

(g) patterning the second photoresist layer to form a second mask pattern defining the second feature;

(h) etching the dielectric layer using the second photoresist layer as a mask to form the second feature.

13. (Original) A method according to Claim 12, further comprising depositing copper or a copper alloy in the first and second feature.

14. (Original) A method according to Claim 13, wherein the dielectric layer comprises SiO_2 or a low K dielectric.

15. (Original) A method according to claim 12, wherein the wherein the etch chemistry comprises NH_3 .

16. (Original) A method according to claim 12, wherein the wherein the etch chemistry comprises NF_3 .

17. (Original) A method according to claim 12, wherein the etch chemistry comprises N_2O .

18. (Original) A method according to claim 12, wherein the etch chemistry further comprises an inert gas.

19. (Original) A method according to claim 18, wherein the inert gas is selected from the group consisting of He, Ne and Ar.

20. (Original) A method according to claim 12, wherein the etchant comprises one or more of a hydrofluorocarbon, a fluorocarbon, a hydrochlorocarbon, or a chlorofluorocarbon.

21. (Original) A dual damascene method of forming an interconnect structure having a via and a trench, comprising the steps of:

(a) providing a semiconductor wafer comprising a conductive layer that has a dielectric layer thereon;

(b) depositing a first photoresist layer on the dielectric layer;

(c) patterning the first photoresist layer to form a first mask pattern defining the via;

(d) etching the dielectric layer using the first photoresist layer as a mask to form the via using an etch chemistry that comprises a member of the group NH_3 , NF_3 and N_2O ;

(e) removing the first photoresist;

(f) depositing a second photoresist layer on the article;

(g) patterning the second photoresist layer to form a second mask pattern defining trench;

(h) etching the dielectric layer using the second photoresist layer as a mask to form the trench;

(i) depositing copper or a copper alloy in the trench and via; and

(j) etching the copper or copper alloy back to the surface of the dielectric layer.